

Contact to Contacts or Silicide by use of Backside FIB Circuit Edit allowing to approach every Active Circuit Node

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Abstract

Direct measurements, connecting to central circuit nodes without changing the performance of the circuitry are critical in modern FA but often impossible for recent IC technologies. This paper shows two new methods based on FIB backside circuit edit, allowing to reach every circuit node existing on front-end level.

1. Introduction

Following the past decade FIB based Circuit Editing became increasingly important, since it is the fastest and most economic way of modifying a circuitry to evaluate new circuit designs.

Essentially circuit edit (CE) consists of CAD assisted precise placement, milling of access holes, to subsequently cut or reconnect lines on the access hole bottom. In order to perform CE in small recent and future technology shrinks, the requirements are: a fine beam spot, high aspect ratio node access processing and very accurate alignment.

Traditionally a circuit is accessed through the structured front side but obviously lower interconnect levels and poly-silicon are very difficult to access in present high metal stack level processes. In addition, these metal lines typically provide connection to and are located near transistor gates highly susceptible for charging effects as threshold voltage shift. Therefore aligning on those levels during a front side edit is difficult and poses risks to devices.

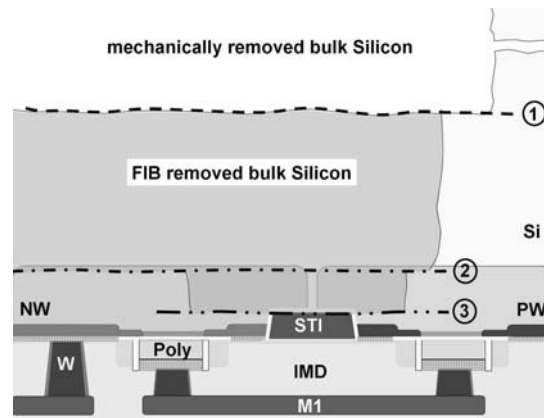


Figure 1: Process Flow of backside CE

An access from the back overcomes the inherent risks of precise alignment on metal or poly lines. A backside edit procedure [1, 2] (Figure 1) starts with a mechanical thinning of the die to 10~40 μ m remaining silicon thickness, indicated with line (1).

Subsequently, a large trench on top of the desired edit region is locally milled down using the FIB tool until the operator stops (“endpoints”) on n-well level. The

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