Novel and Practical Method of Through Silicon FIB Editing of SOI Devices

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Abstract

Circuit edit techniques have been developed for silicon-on-insulator (SOI) devices using a coaxial photon-ion column. Novel trenching, navigation and milling methods, utilizing sub pico-Amp beam currents provide enhanced capability for editing devices with decreased geometries including buried (Box) thickness. Flat trenches 200x200µm were obtained using real time optical fringe monitoring with 125nm accuracy with 950nm λ and FIB bit map milling to adjust for parallelism to the ILD0. This bit map milling technique controlled the etch rate to maintain trench flatness by correlating the optical fringes to the bit map grayscales to vary the dwell time of the ion beam across the trench floor. Through highly accurate, CAD directed beam deflection control, beam placement accuracy in the sub 20nm regime can readily be accomplished, sub pA beam currents provide ultra-controlled etch rates and high aspect ratio (HAR) capability. Complete process definitions, techniques and results are reported. These techniques have proven successful in circuit edit below 90nm, and are expected to meet future technology circuit edit requirements down to 45nm.

Introduction

The cost of and time for mask reworking is increasing with decreasing technology nodes. Circuit edit of semiconductor devices is a great benefit [1] and its value to the IC industry need not be lost. As the number of IC metallization levels has increased the difficulty of FIB editing has increased. Then with the advent of flip-chip packaging it became obvious that through silicon editing was required for IC development to continue. On flip-chip and planarized front side devices navigation to the circuit node of interest is difficult because the FIB can only see surface features.

SOI (silicon-on-insulator) CMOS devices unlike traditional CMOS devices comprise a layer of silicon dioxide, buried oxide (BOx), which insulates the bulk silicon from the active silicon. Charge sensitivity is higher in SOI devices where discharge paths are for the most part unavailable through the BOx unlike the bulk silicon in regular CMOS processes [4].

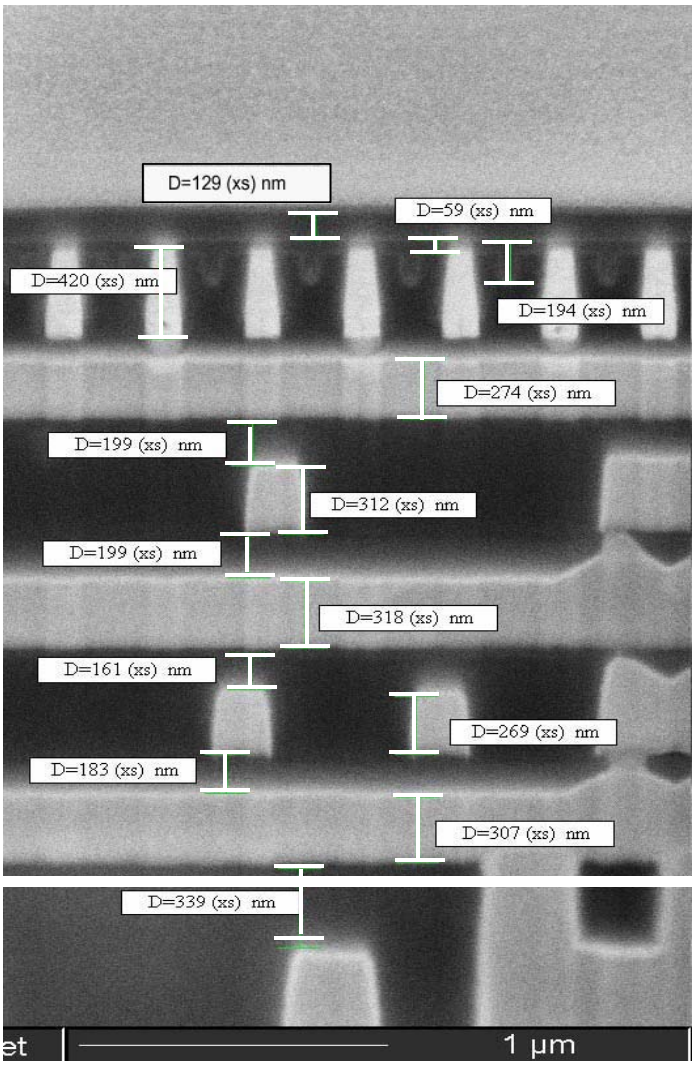

Figure 1.Cross-section image to obtain layer thickness information of Inter layer metal and dielectrics. The information helps determine etch rate and dosage

Charging on the BOx can alter the threshold voltage (V_T) of charge sensitive gates [3]. Traditional CMOS through silicon circuit edit recipes will not work on SOI devices due to lack of n-well and shallow trench isolation (STI) structures in the bulk