

Role of Circuit Edit in Post-Silicon Debug and Diagnostics

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Abstract: Circuit edit is a well-known step in the validation of first silicon and is also used to partially validate next generation designs. The use of circuit edit remains viable even with the increasing design and process complexities of ICs. However, by implementing some design and process changes its value can be improved.

Keywords: Silicon debug, circuit edit, FIB, design validation, Design for Diagnostics

Introduction: The challenge of producing a working first prototype is becoming increasingly complex as technology moves into deeper sub-micron architectures. The use of circuit editing instruments has established itself as common practice for many companies to reduce their number of mask cycles. This is readily justified by the high cost of masks — circuit edit (CE) has significant return on investment (ROI) for pre-second mask validation. The reason for most first silicon designs needing rework is that they go to tape out and fabrication before all functional checks are completed. Performing complete functional checking on a design takes too long and becomes very costly to perform. When a SOC design fails it is generally due to IP that has not been validated in silicon from the fab process that was used for its creation.

Circuit Edit Technology: To date, a focused ion beam (FIB) instrument has generally been used to physically edit the circuitry previously fabricated into the silicon. The original concept for creating a circuit edit tool proposed using electron beams [1]. A focused ion beam was eventually concluded to be much more controllable and efficient. A FIB instrument, by virtue of being able to perform cuts and deposits on silicon, may appear to be a “Fab-in-a-Box”. This is not true, however, due to some specific technological limitations. One of the limitations of a FIB technology is that it cannot create transistors – as a result, the scope of its ability to re-create complete silicon circuits is very limited. Furthermore, FIB instruments cannot deliver the precise via resistivity that the fab can. In addition, the capacitance the FIB yields is generally greater than that produced during final fabrication because the FIB traces are working in and around the fabrication as per the designed layout. Despite these limitations, however, the

FIB and the fab face many of the same challenges. For years FIB circuit edit efficiently addressed design modifications for designs fabricated using Al and SiO₂. The advent of CMP (Chemical Mechanical Polishing) presented a new challenge; however, since FIB imaging relies upon the presence of some sort of surface topography in order to image the surface. This challenge was eventually overcome by incorporating a conventional optical light microscope co-axial to the FIB [2] and by the implementation of a precision electronic deflection stage [3]. These new tools, when used along with fabrication of seeker holes in the planarized surface, [4] are sufficient to address the navigational issues caused by the loss of topographic guides as the result of CMP. The introduction of new materials has also presented new roadblocks to efficient circuit edit. Although low-k dielectrics have been the most challenging in the fab, the bigger issue for circuit edit has been the milling of copper metallization. [5] {Fig 1. shows FIB exposed copper dummy fill metal within porous carbon-doped oxide (CDO) low-k}. Because copper grains etch none uniformly the removal of copper is not uniform; further, removed copper tends to migrate elsewhere, causing shorts. The solution has been chemical — a chemistry, which evens out the removal of copper and keeps it bound up as a non-conductor when it lands elsewhere. Further with the reduction of dielectric k constant the chemistry must also be a kind of replacement therapy so the low k dielectric is not lost.