

Backside E-Beam Probing on Nano Scale Devices

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Abstract

IC debug with E Beam Probing is presented in an innovative application accessing the active device directly from chip backside after FIB preparation. The potential of this approach in nanoscale and gigahertz dimensions is evaluated.

1. Introduction

Measuring timing and voltage signals inside an integrated circuit (IC) is critical to debugging new devices. E-beam probing (EBP) on front side devices has been very useful for over two decades [1]. For measuring signals below the top metal layers, probe pads could be made using a focused ion beam (FIB) when lower metal was accessible. This approach usually fails in technologies with high metal stacks as the probability of accessibility to lower metal layers decreases with the increase in the number of metal layers. Optical techniques such as the Laser voltage probing (LVP) and time resolved photon emission (TRE) were introduced for through silicon probing [2]. However, with all optical techniques the lateral resolution is limited to a fraction of the wavelength.

Transition of IC packaging to flip chip technology has necessitated the need for new set of tools or methodology for design debug and failure analysis. It is now possible to perform EBP from the backside on exposed active transistor areas [3, 6]. Recent investigations have shown that removing the bulk silicon and exposing the shallow trench isolation (STI) has little influence on circuit performance [4, 7]. Procedures emphasizing highly controlled etch rates were utilized for trenching through bulk silicon [5].

This paper shortly reviews the necessary sample preparation using the Credence OptiFIB and presents experimental data to discuss the physical signal generation and to evaluate the capability of this methodology with respect to V_{dd} / signal scaling, long loop length measurement stability and timing accuracy. Furthermore the theoretical performance limitations of the present EBP systems are compared to optical backside analysis tools and possible system improvements and future challenges are discussed.

2. Backside Sample Preparation

The backside sample preparation starts with depackaging and mechanical thinning using either global lapping tools or more localized grinding tools to reduce the remaining silicon

thickness to less than 40 μ m in the relevant chip area (marked with line 1 in Figure 1). The mechanical thinning has to be completed with a very accurate mechanical fine polish to enable the following FIB preparation. Subsequently, a large trench covering the area of interest is locally milled down using the FIB tool until the operator stops (“endpoints”) on the n-well (NW) level. The trench bottom at this stage is marked with line (2). From this trench floor one or more small windows down to the STI level can be opened.

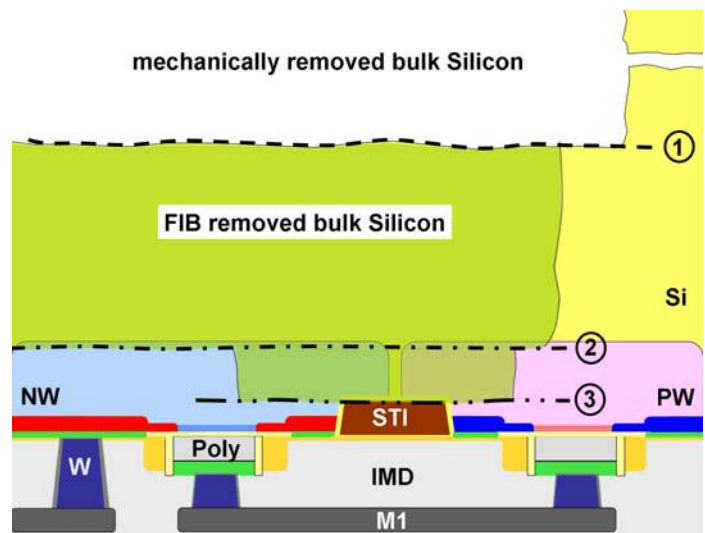


Figure 1: FIB backside preparation flow

The finally remaining active chip area underneath the opened STI window (below line 3) is then reduced to the technologically determined height of the STI shapes (approximately 300 to 400 nm with the different bulk / STI processes of the utilized samples) [4, 7]. Presuming an adequate mechanical thinning the necessary FIB preparation will take less than two hours.

3. Theoretical Signal Generation

In Figure 2 we see a cross section through an n-FET structure as it would appear after the FIB trench down to STI level. As reported in [4, 7] the functionality of the transistor, or the IC in general, is not critically effected by this preparation. The estimated penetration depth of the gallium ions is below 50nm and with a remaining layer thickness of more than 300nm the