Effects of Backside Circuit Edit on Transistor Characteristics

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Abstract

Backside circuit edit techniques on integrated circuits (ICs) are becoming common due to increase number of metal layers and flip chip type packaging. However, a thorough study of the effects of these modifications has not been published. This in spite of the fact that the IC engineers have sometimes wondered about the effects of backside circuit edit on IC behavior. The IC industry was well aware that modifications can lead to an alteration of the intrinsic behavior of a circuit after a FIB edit [**1**]. However, because alterations can be controlled [**2**], they have not stopped the IC industry from using the FIB to successfully reconfigure ICs to produce working "silicon" to prove design and mask changes. Reliability of silicon device structures, transistors and diodes, are investigated by monitoring intrinsic parameters before and after various steps of modification.

Introduction

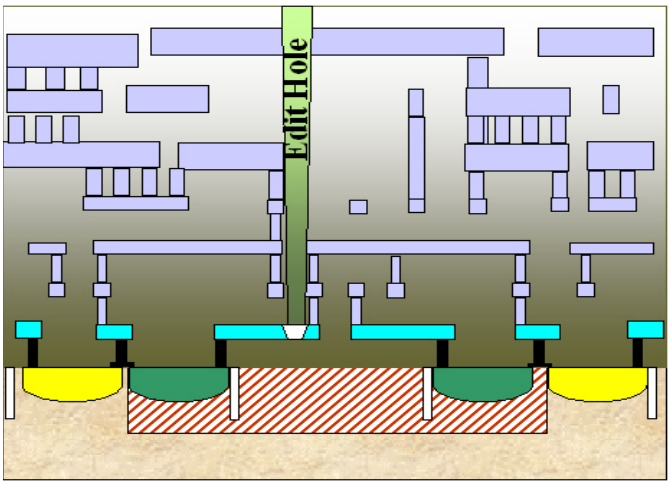
The increase in density of advanced process devices and the decrease in interlayer material thickness have again increased the difficulty for the FIB community to produce successful circuit edits. Circuits are modified not only to produce prototypes during first silicon debug but they are also edited for engineering samples to be distributed for system validation and software development. Therefore, accuracy and reliability of the edit becomes very important—it must last more than a few hours; it needs to last weeks if not longer. Front side studies on affects of circuit edit ion beams on device parameters such as threshold voltage (V_T) have been published [**3, 4**][1]. It does need to be noted that dynamic affects of backside editing has been investigated at Intel [**5**] and the Technical University of Berlin [**6**]. But these have not investigated transistor I-V curves.

There are some fundamental differences between backside and front side circuit editing. For example, the edit incorporates cutting an M1 line on a 6 metal layer 0.13 µm Copper process. Two power planes and one dummy structure from the topside cover the M1 line (Fig 1a). From the backside there is some dummy diffusion and poly covering the M1 (Fig 1b).

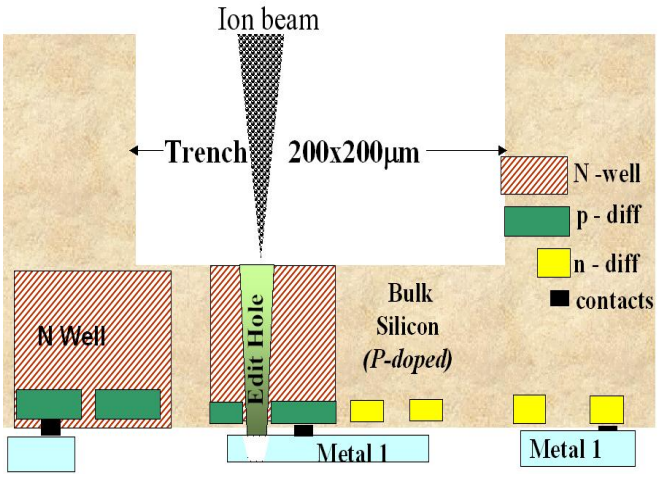
[1] It might be that when gate dielectric was thicker there was more of an issue due to charge injection into the dielectric and as this dielectric has gotten thinner it becomes pretty much self healing.

Starting from sample preparation to the completion of the edit a backside circuit edit goes through some different process steps compared to a front side edit. The impact of each of these backside edit steps is studied and will be presented in this paper:

1. DUT thinning
2. n-Well exposure
3. STI exposure
4. Through silicon editing



(a)



(b)

*Figure 1: (a) Typical frontside edit process on a standard CMOS process [**8**]. (b) Typical backside edit process on a standard CMOS process [**9**].*