Deposition of Narrow, High Quality, Closely Spaced, but Isolated Conductors

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Abstract

Developed procedures to deposit narrow (≤100nm), closely spaced, low resistance conductors which exhibit good electrical isolation are demonstrated. The process parameters which limit how narrow a line can be deposited and the methods used to work-around these are discussed. For these depositions, 3pA ion beam current was used with a $Mo(CO)_6$ precursor chemistry. The deposition method minimized the incorporation of non-conductive precursor by-products. To isolate adjacent conductors, a copper etch Credence FIB chemistry was used. The advantages of this procedure over the common practice when XeF_2 chemistry is used is also discussed and demonstrated.

Introduction

During some process characterizations such as nano-probing of memory cells, a probe structure is created (Fig. 1a) [1]. This structure consists of high quality dielectric, low resistance vias and conductors connecting transistor elements to probing pads. This characterization activity measures I-V curves of cell transistors, which requires operating current (~200μA) through the deposited conductors. This operating current requires not only low resistance conductors but with small dimensions for instance those required for ≤90nm process technologies these conductors must also be narrow and minimally spaced (≤100nm). This creates a significant challenge during the deposition over-spray clean-up step that is necessary to obtain electrically isolated conductors. These narrow, high quality, closely spaced but isolated conductors are also important in TeraHz detectors (Fig. 1b) [2].

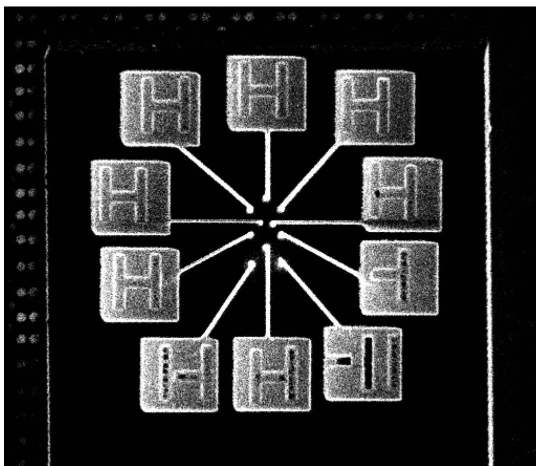

Figure 1a

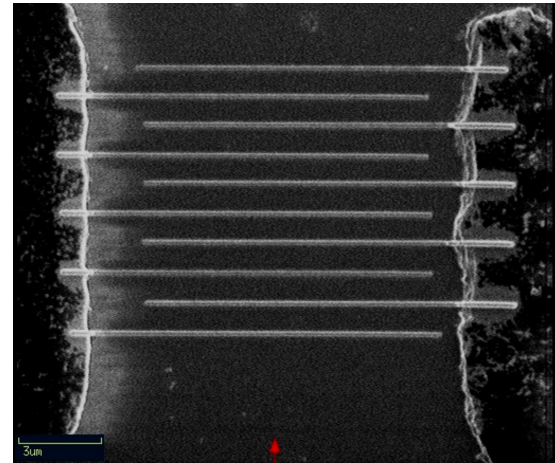

Figure 1b

Figure 1a: FIB micrograph of "wagon wheel" structure used to probe SRAM cells for process characterization. Figure.1b: TeraHz detector structure. Both structures require deposition of narrow, high quality, closely spaced, but isolated conductors.

In this work, we demonstrate the use of $Mo(CO)_6$ for FIB deposition of thin, high quality, narrowly spaced isolated conductors. To minimize lateral broadening of the conductor lines, a one pixel wide line scan (OLS) FIB operation was applied. This approach allows a reduction of the width of the deposition down to the natural limit defined (in general) by the beam spot size and precursor activation area diameter for the given precursor at a given substrate. This OLS approach also simplifies control over deposited conductor quality (conductivity). The primary quality control factor is deposition yield which was controlled with the beam scan speed. We were able to optimize the process parameters very close to those when deposition turns into etching, however the deposition mechanism still dominated over etching. Further, we compare quality and geometry of thin conductors deposited under these conditions with those which were deposited when the deposition was highly dominating over etching. We offer a recipe for over-spray removal after conductor deposition which allows isolation of narrowly spaced conductors from each other without damage to the dielectric in between the conductors. We compare this recipe with the common practice when the over-spray is removed using XeF_2 chemistry.

Experimental setup

All the experiments were performed on a Credence P3X FIB Circuit Edit system. Thin conductors were deposited using 3pA beam current (collimated mode) on the SiO_2 substrate in between Aluminum traces that are connected to an external pin out to perform resistance measurements. To avoid high