FIB backside circuit modification at the device level, allowing access to every circuit node with minimum impact on device performance by use of Atomic Force Probing

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Abstract

Direct measurements of circuit node signals without changing the performance of the circuitry are essential in modern FA but often impossible for recent IC technologies. This paper shows new methods, based on FIB backside circuit edit, allowing access to every existing circuit node at the device level, and discusses options for probing and discrete characterization.

Introduction

Throughout the whole development of Failure Analysis (FA) discrete transistor characterization and probing of inner circuit nodes has always been essential. As long as the number of metal layers was moderate Focused Ion Beam (FIB) tools were widely used to create electrical contacts to targeted circuit nodes [1] through the frontside of the chip. But due to technology innovation and Flip Chip packages the direct access from the structured frontside to the inner circuit nodes and especially to the transistor level is mostly blocked [2, 3].
For this reason, optical analysis tools, such as Time Resolved Photon Emission or Laser Voltage Probing, were developed and are widely used. These tools allow load-less probing of inner circuit nodes through the thinned chip backside and offer very high bandwidth. But because of the limits of optical microscopy the lateral resolution is no longer sufficient to resolve the smallest transistors on recent technologies.
For the characterization of single transistors, the most common procedure is to take away all metal layers down to the tungsten contacts by use of parallel lapping. After that, FIB pads may be deposited, followed by electrical characterization at a regular probe station. Alternatively, a SEM probe station can be used to characterize the suspected transistors. During the past years Atomic Force Probing (AFP) was developed to a necessary level of stability to provide a relatively fast solution, where no FIB deposition and no vacuum based SEM system are needed for discrete device characterization. The biggest disadvantage of these methods is that they require the physical destruction of the circuitry. If the root cause was located in the metal stack or can not be found amongst the suspected transistors, the operator does not have a second chance.
This paper shortly reviews the application of AFP from the chip frontside, and then reviews the FIB backside circuit edit (CE) procedure, including all necessary preparation steps. The main topic is direct probing and single transistor characterization from the chip backside by use of a regular probe station and AFP.
The paper shows how a new backside Circuit Edit (CE) procedure, named Contact to Silicide (CtS) can be used to contact any inner circuit node. This method offers a way to do probing and most of the desired single transistor characterization without destroying circuit functionality.
To speed up the analysis routine, classical FIB pads can be avoided by the use of AFP. This also minimizes the impact on high frequency device performance, allowing high speed testing and various discrete measurements on the same DUT.
Experiments on ring oscillators (RO) are presented to demonstrate general functionality and to elaborate on the limitations of these methods.

AFP on parallel polished samples

Figure 1 shows the cross section through a readily prepared DUT, illustrating the general idea of AFP. The sample has been reduced to the device layer including the tungsten plugs.

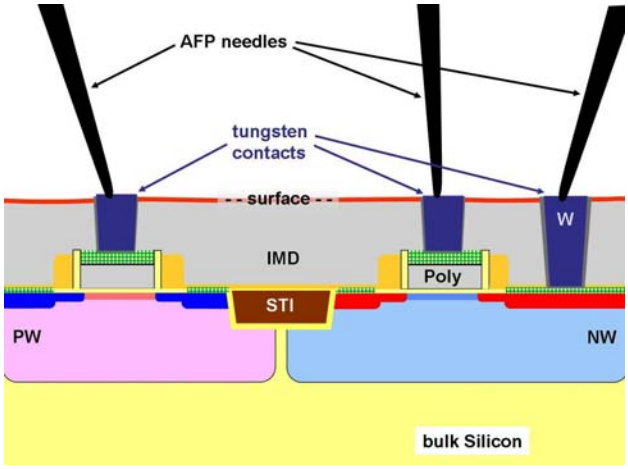

Figure 1: AFP on lapped frontside sample