

Novel Flip-Chip Probing Methodology Using Electron Beam Probing

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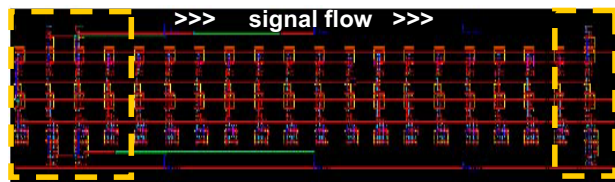
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1. Introduction

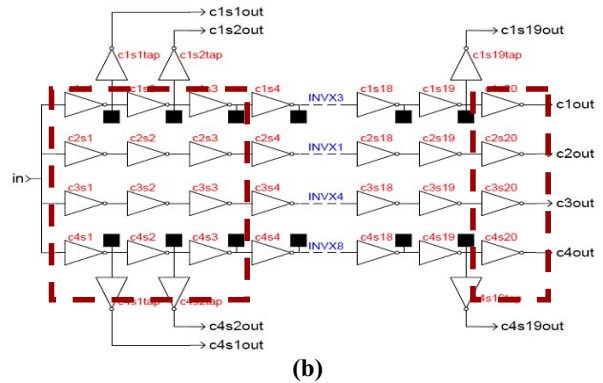
The measurement of timing and voltage signals inside integrated circuits (IC) is critical to debugging new devices, to failure analysis of advanced devices, validating new IP (intellectual property) in new silicon, etc. E-beam probing (EBP) has been very useful for front side devices for over two decades [1]. For measuring signals below the top metal layers, probe pads are made using a focused ion beam (FIB) where lower metal was accessible. This approach usually fails in technologies with high metal stacks as the accessibility to lower metal layers decreases with increasing number of metal layers. Optical techniques such as the Laser voltage probing (LVP) was introduced for through silicon probing of flip chips [2]. However, optical techniques have limited lateral resolution with infrared (IR) light unless a solid immersion lens (SIL) is employed [3]. Increasing migration of ICs to flip chip packaging has necessitated the need for a new tool set or methodology for design debug and failure analysis. It is now possible to perform EBP from the backside on exposed active transistor areas [4,7]. Recent investigations have shown that removing the bulk silicon and exposing the shallow trench isolation (STI) has negligible influence on circuit performance [5]. Procedures emphasizing highly controlled etch rates were utilized for trenching through bulk silicon [6]. This paper introduces data taken from a flip chip using an IDS 10K+ E-beam Prober (EBPr). The samples are thinned using an Allied Hi-Tech polishing wheel and the Credence OptiFIB. The investigation utilized the capability of the EBPr to acquire both repeating (clocks) and non-repeating signals at various: supply voltages, loop lengths frequencies.

2. Experimental Setup

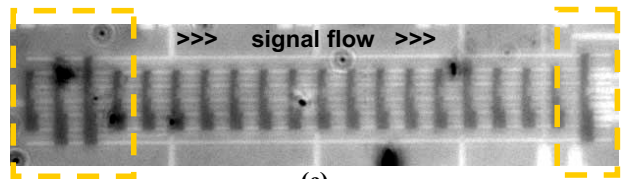
Measurements were done on a test chip, fabricated in a TSMC 180nm, CMOS technology. For maximum flexibility in choice of input signal, the region of interest contained a group of 4 differently designed inverter chains consisting of 20 stages in each row (Fig. 1). The test chip was tested for functionality before starting any sample preparation.



(a)



(b)



(c)

Figure 1: (a) Physical layout (b) Schematic (c) Optical Image of the inverter chain, with FIB opened areas indicated by dashed box

The sample preparation began with global mechanical thinning of the die down to 40 μm remaining silicon thickness using a polishing wheel. The last polish was done using a 0.25 μm grit paper; the final polish is extremely critical before using the FIB for local thinning. A good polish minimizes pitting during local thinning/trenching [9]. A coaxial photon-ion circuit edit FIB (Credence OptiFIB) was used to locally thin down a 50x200 μm area on the device. The device CAD layout is locked to the optical image of the device. The FIB used a 20nA beam at 30kV to thin down to 7 μm remaining silicon, and then the remaining silicon was removed using a 4nA beam at 15kV. Using advanced fringe analysis techniques on a coaxial photon-ion system allowed us to maintain planarity < 1 μm during thinning [6]. It is very important to maintain good planarity of the trench for all subsequent operations. The area was uniformly thinned down to the n-wells using the ion beam (Fig. 2).

