

# New Circuit Edit and Probing Options directly to FET Device on Ultra Thin Silicon Backside processed by Focused Ion Beam

R. Schlangen<sup>\*</sup>, U. Kerst, C. Boit

*Department of Semiconductor Devices, Berlin University of Technology  
Einsteinufer 19, Sekr. E2, D-10587 Berlin, Germany*

R. Jain, T. Malik, T. Lundquist

*Credence DCG, CA 94089-1138 Sunnyvale, USA*

---

## Abstract

Direct measurements, connecting to central circuit nodes without changing the performance of the circuitry are critical in modern FA but often impossible for recent IC technologies. This paper shows three new methods based on FIB backside circuit edit, allowing to reach every circuit node existing on front-end level.

---

## 1. Introduction

Following the past decade FIB based Circuit Editing became increasingly important, since it is the fastest and most economic way of modifying a circuitry to evaluate new circuit designs.

Essentially circuit edit (CE) consists of CAD assisted precise placement, milling of access holes, to subsequently cut or reconnect lines on the access hole bottom. In order to perform CE in small recent and future technology shrinks, the requirements are: a fine beam spot, high aspect ratio node access processing and very accurate alignment.

Traditionally a circuit is accessed through the structured front side but obviously lower interconnect levels and poly-silicon are very difficult to access in present high metal stack level processes. In addition with the growing importance of flip chip technology this more and more enforces new methodologies.

An access to the chip from the backside overcomes most of these problems. Flip chip DUTs can mostly be prepared without time and cost intensive repackaging and the poly and lower metal layers can be accessed more easily through electrically unused chip area (Shallow Trench Isolation - STI, surrounding every active transistor area, and dummy diffusions).

## 2. FIB Sample Preparation

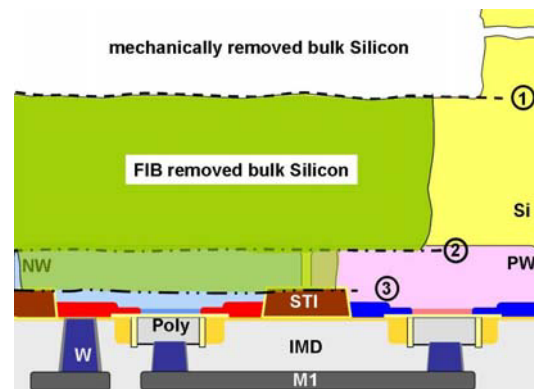


Figure 1: Process Flow of backside CE

The FIB backside preparation procedure [1, 2] is depicted in Figure 1. It starts with the mechanical thinning of the die to 10~40 $\mu$ m remaining silicon thickness, indicated with the dashed line (1).

Subsequently, a large trench on top of the targeted chip area is locally milled down using the FIB tool, with Xenondifluorine assisted etch, until the operator stops ("endpoints") on n-well level. With the use of the in-situ IR optics of the OptiFIB the operator has a direct

---

<sup>\*</sup> Corresponding author. Schlangen@mikro.ee.tu-Berlin.de  
Tel: +49 (0) 30 314 25406; Fax: +49 (0) 30 314 25526